

Research on the Controller of Cycloconverter-fed Salient Synchronous Machine

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Abstract

A new full digital controller is developed in this paper, which is designed for implementing the vector control of a cycloconverter-fed salient synchronous machine. This controller is composed of an advanced DSP and a FPGA. Vector control algorithm is accomplished by DSP. The functions of generating triggering pulses and changeover control are implemented by FPGA. The vector control system of 2.2kW 3-phase salient synchronous machine has been achieved based on this controller. Design details and experimental results are presented in this paper.

Keywords: Salient Synchronous Machine, Cycloconverter, Vector Control, DSP&FPGA

1. Introduction

The status of cycloconverter-fed salient synchronous machine is very important in the applications of high power and low speed drive, such as mining hoist and rolling mill. Full digital controllers and software are the most important core in the whole system. According to the latest research results on theory, some new control methods can greatly improve the performance of cycloconverter. But the calculation and communication capabilities of conventional controllers are not enough. Therefore, research on new controller and corresponding software is necessary in view of the costing.

A new digital controller is developed in this paper, which is applied in the vector control system of a cycloconverter-fed salient synchronous machine. Advanced DSP and FPGA chips are both used. Complex algorithm is implemented by DSP. Functions of generating triggering pulses and changeover control are implemented by FPGA. The vector control system of 2.2kW 3-phase salient synchronous machine is achieved based on this controller. Design details and experimental results are also given to show the validity of the proposed controller.

2. Cycloconverter

2.1 1-Phase Cycloconverter

1-phase cycloconverter is shown in Fig. 1, which includes two inverse-parallel 3-phase bridges. The direction of the output voltage is also indicated in Fig. 1. Bridge changeover control strategy relies on the correct state signal of bridge, on or blocking.

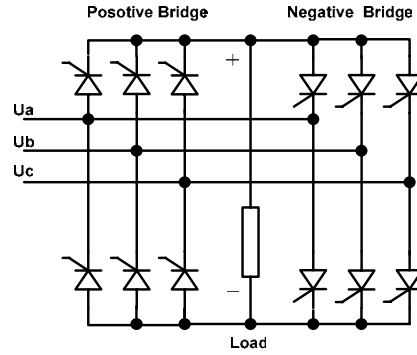


Fig. 1. 1-Phase Cycloconverter

2.2 3-phase cycloconverter

3-phase to 3-phase cycloconverter is composed of three 1-phase cycloconverters. Its structure is shown in Fig. 2. The 3-phase output voltages are symmetrical. Star connection is preferred in high power applications. Only the 6-pulse non-circulating current cycloconverter will be focused on in this paper.

3. Structure of Control System

The structure of control system is shown in Fig. 3. The algorithm of vector control is implemented by DSP chip TMS320LF2407A, which is delivered by TI. At the same time, electrical signals of stator and excitation windings are collected by A/D converters integrated in DSP. The communications between DSP and PLC are accomplished by RS232.

The FPGA chip SPARNTAN II XC2S200 delivered by Xilinx generates the triggering pulses and implements bridge changeover control. Another FPGA chip of the same type collects the data of the rotary encoder, calculates the rotor position and speed, and sends them to DSP.

Both two FPGA chips are used as programmable peripheral chips of DSP. The 16-bit data bus and 16-bit address bus are shared by DSP and FPGA chips.

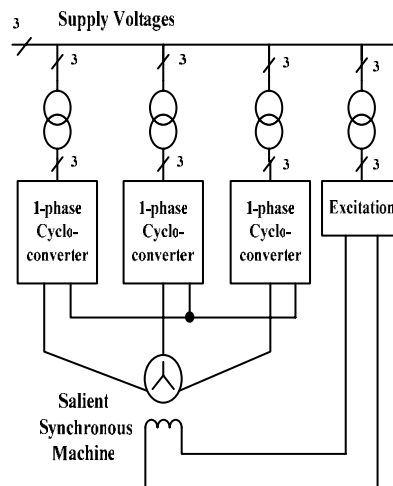


Fig. 2. 3-Phase Cycloconverter

4. Pulses Generator and Bridge Changeover Controller

4.1 Characteristic

The characteristics of triggering parts of cycloconverter are described below.

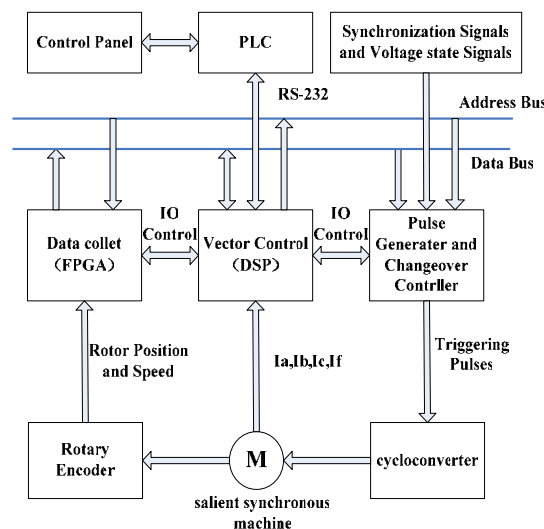
The number of thyristors to be triggered is large. The relationships between pulses and the phase of supply voltages are close. The sequence of triggering is fixed.

The changeover control also needs pulse logic signal to be supported as logic input.

According to the characteristics above, the triggering pulses generator and changeover controller can be designed independently as part of a cycloconverter controller. The full digital implementation is preferred.

4.2 FPGA Design

There are mainly two methods to generate triggering pulses in the conventional scheme. One is using several single microprocessors, because the number of IO interfaces in a single microprocessor is usually not enough. Another one is designing complex digital circuits.

**Fig. 3.** The Structure of System

DSP, which is used to implement vector control algorithm, is also used to implement changeover control in conventional digital control system.

In this paper, the FPGA is chosen to generate pulses and control changeover. Comparing to conventional schemes, the advantages of FPGA include 3 aspects. At first, FPGA IO resource is abundant. Secondly, real time control needs faster digital circuits than before, and the performance of FPGA to design sequential logic circuits is good.

At last, the development environment of FPGA is easy to use. The difficulty and time cost for hardware design are decreased greatly.

The structure of FPGA is shown in Fig. 4. This FPGA is the pulses generator and changeover controller in design. Several function modules are included. Details about each module will be introduced hereinafter.

4.3 Design of oscillator clock

40MHz crystal is used as the external clock of FPGA, which is near the clock of DSP.

The precision of triggering angle depends on the clock of digital counter in FPGA. If 40MHz is chosen, the precision can reach 0.00045 degree according to 50Hz supply voltages. For timing, this precision is so high that the length of counter in FPGA must be greater. So FPGA will be short of resources.

In fact, we chose 156.25kHz oscillator clock, which is 40MHz divided by 256, to trigger all the modules related with motor control. The precision can reach 0.115 degree. 40MHz oscillator clock is only used to trigger communication module related with DSP.

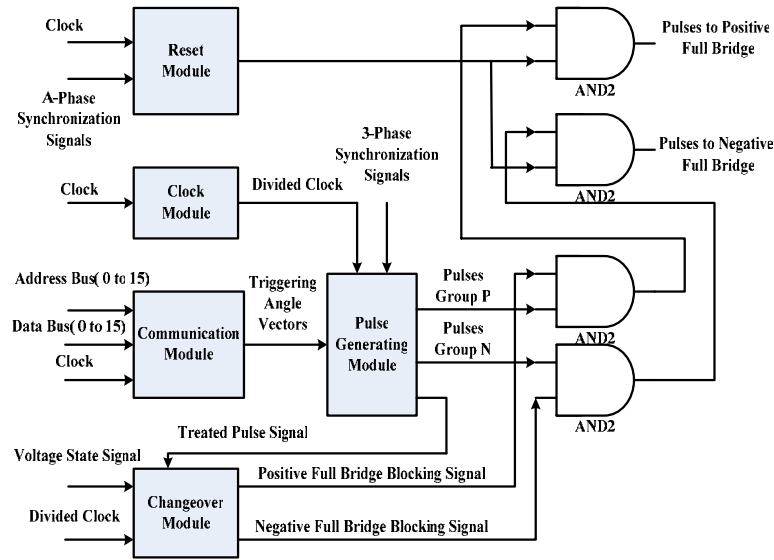


Fig. 4. The Structure of FPGA Design

4.4 Communication Module

The bidirectional communications are achieved via the data bus and address bus of DSP. Since FPGA is a programmable peripheral device, DSP can use different addresses to distinguish different triggering angles among 3-phase output voltages and excitation voltage. At the same time, more complex control functions can be accomplished by flexible address setting mode.

4.5 Reset Module

This module implements auxiliary functions, which can send block signals to the output after FPGA is reset. The block signals will just maintain 0.8S. This module can also make it certain that the first triggering pulse generated by FPGA always be related to the synchronization signal of input voltage of phase A. Thus, the pulses will not be in chaos when DSP and FPGA are turned on.

4.6 Pulse Generating Module

This module uses 3-phase voltages to synchronize triggering pulses. In Fig. 5, syn_a, syn_b, syn_c are the synchronization signals of 3-phase supply voltages, U_a, U_b and U_c. They are already delayed for 30 degrees. Syn_/a, syn_/b, syn_/c are the inverse synchronization signals of syn_a, syn_b, syn_c. Each synchronization signal is related to only one thyristor in bridge. The relationships between synchronization signals and thyristors in positive bridge are shown in

Fig. 5. For example, the pulses generated by syn_a are only sent to the 1st thyristor.

This kind of synchronization mode can be regarded that FPGA synchronizes one time each 60 degrees of supply voltages,.

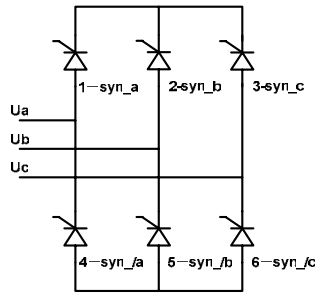


Fig. 5. Synchronization Signal and Corresponding Thyristor

The principle of generating pulses is shown in Fig. 6. The rising edge of each synchronization signal (input signal EN in Fig. 6) enables a counter. The vector output of counter is compared with the angle vector, which is sent from DSP. If the former is larger than the latter, the pulse will be generated immediately.

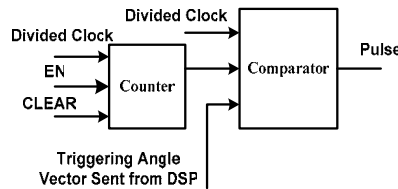


Fig. 6. Principle of Generating Pulses

Because the length of the counter in FPGA is enough to time 180 degrees (10mS), the look-up tables of triggering commands, which is used in some conventional triggering methods, has been removed.

In this system, the triggering alpha vectors from DSP only include three positive bridges triggering alpha vectors in cycloconverter. That is to say, only using these triggering alpha vectors, the output 3 -phase voltages must be all positive. So three negative bridges triggering alpha vectors should be calculated by FPGA in real time, the formula is listed below.

$$\alpha_{negative} = 180^{\circ} - \alpha_{positive} \quad (1)$$

The function of adjusting width of pulses is achieved by following modules, which is not discussed here.

4.7 Changeover Control Module

In this scheme, the voltage between anode and cathode is used to detect the state of thyristor. The optocoupler circuits can transfer supply voltage analog signals to the voltage state digital signals, which are used by FPGA. However, when the thyristor is blocking, the voltage between anode and cathode is just the supply voltage. If the input voltage is near zero, the output of optocoupler circuits will be similar with the output when the thyristor is on, and the age state signal must be false. These faults should be removed.

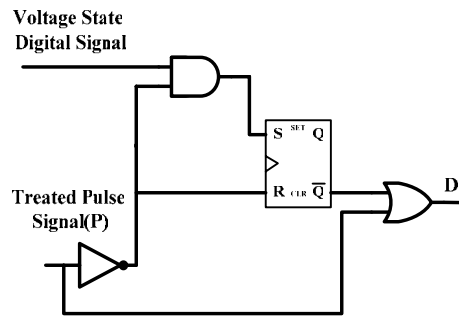


Fig. 7. thyristor state judgment circuit

The structure of thyristor state detecting circuit is shown in Fig. 7. The triggering pulses and the voltage state signal are both used as logic inputs

The treated pulse signal P in Fig. 7 is described below. The example is the signal P of the 1st thyristor in Fig. 5. When the triggering pulse of the 1st thyristor comes, P will change to 1. P will change to 0 on the moment when the pulse of the 2nd thyristor comes. The 1st and 2nd thyristors are both in the upper legs and it is regarded that the 2nd will be on after the 1st is blocking. The rest treated pulse signals are all generated by means of this principle.

If the output signal D of circuits shown in Fig. 7 is 1, it is indicated that the corresponding thyristor is blocking. The state signal DP of positive bridge can be achieved by AND logic function. As Fig. 5 shows, we can only use 3 thyristors, the 1st, 2nd and 3rd, to detect the state of positive bridge. If 3 thyristors in upper legs are all blocking, we can get the state signal DP of positive bridge is 1. In this way, the state signal DN of negative bridge is easy to get. When DP and DN are both 1, changeover control will work.

The state of DP=1 and DN=1 must last for a while so that the positive bridge and negative bridge are both blocking in theory. This time can be called “first delay”. In this paper it is set to be 0.2mS. When the first delay is over, the pulses of the previous working bridge should be blocked at once. But the other bridge should not be turned on at the same time. In order to avoid short circuit, the blocking state of all pulses must last for another moment named “second delay”, which is also set to be 0.2mS. After the second delay, it is safe to turn on the other bridge. The process of changeover is over.

5. Software Design

The control strategy of this design is rotor-flux-oriented vector control which is shown in Fig. 8.

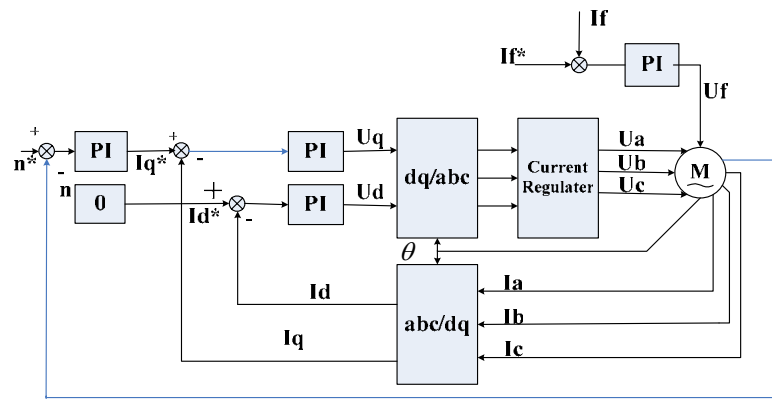


Fig. 8. Rotor-Flux-Oriented Vector Control

FPGA pulse generator and changeover controller is independent from vector control algorithm of DSP, except the triggering angle vectors sent from DSP. So the capacity of DSP can be sufficiently used.

The average interval between triggering of the six thyristors in full bridge is 3.3mS. But the triggering angles are varying all the time, that is to say, the interval between triggering are also varying. If DSP sends a group of angle vectors every 3.3mS, the effect of time constant produced by controller will be more obvious. The control stability will be decreased. So it is necessary to reduce the time cost of vector control algorithm. The angle vectors, which are received by FPGA, should be as latest as possible. In this design, the cost time of one cycle is set to be 2mS.

6. Experimental Results

The vector control of 2.2kW salient synchronous machine has been achieved based on a new developed controller in this paper. The experimental results are given to show the validity of the proposed controller. DC generator is used as torque load of synchronous machine. The supply voltage is 55V (line voltage).

Fig. 9 shows the stator voltage and current waveforms of synchronous machine. The running frequency is 15Hz. The torque load is light. The upper three waveforms are stator 3-phase voltages. The lower is the current of phase A. In Fig. 10, the running frequency is 5Hz. The torque load is light. The waveform marks are same as Fig. 9.

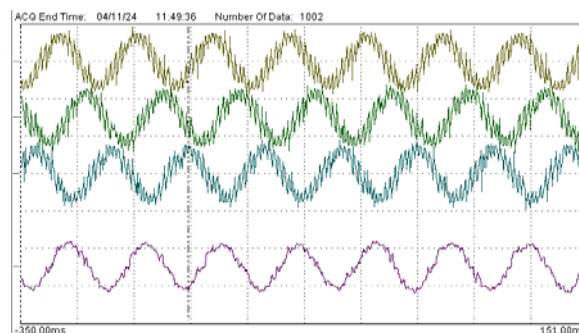


Fig. 9. Waveforms of Stator Running at 15Hz

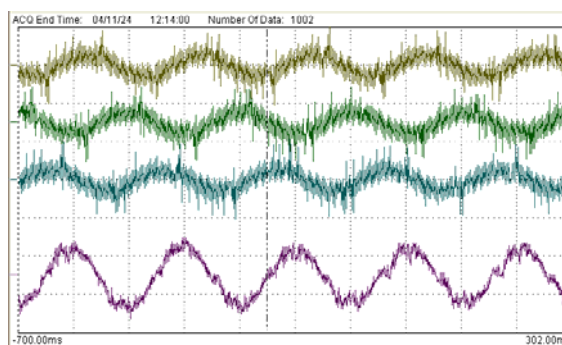


Fig. 10. Waveforms of Stator Running at 5Hz

The detailed experimental results and corresponding analysis will be introduced in other papers.

7. Conclusion

The controller developed in this paper has avoided the disadvantages of conventional schemes by using advanced FPGA and DSP chips. The triggering pulses generator and changeover controller have been integrated in FPGA. They are also independent of vector control algorithm in DSP. Thus both the efficiency and stability of controller are increased.

Experimental results have been achieved by the vector control system of 2.2kw cycloconverter-fed salient synchronous machine, which proved the validity of the proposed controller.

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